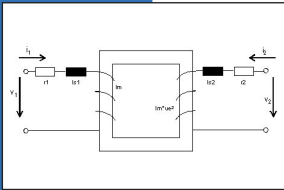
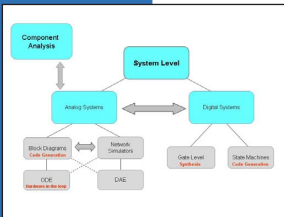
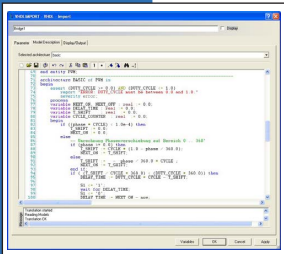
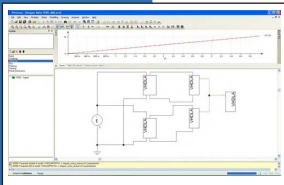


Introduction into VHDL-AMS



```
entity transformer port (
  a: in real;
  b: out real;
  c: in real;
  d: out real;
end entity transformer;

architecture structure of transformer port (
  a: in real;
  b: out real;
  c: in real;
  d: out real;
end architecture structure;
```

Simulations represent a major part of the development process. In addition to the ability of describing and analysing the system to be developed, criteria such as model exchangeability, handling of abstraction levels and automated design generation are essential.

With VHDL-AMS a model description language exists, standardized by the IEEE that is suitable for describing and simulating analogue, digital and mixed-signal systems. A significant advantage of VHDL-AMS lies in the fact that both control algorithm and the system to be controlled, can be described in a convenient way. The considered systems may belong to different physical domains such as electrical, mechanical, thermal, hydraulic etc..

Within the scope of a 2-day training course, the basics of VHDL-AMS are explained and demonstrated as practical examples. The main topics of the training course are:

- Basics of system simulation
- Basic concepts of VHDL-AMS
- Modelling of analogue systems
- Modelling of digital systems
- Selected modelling problems

The exercises are carried out by using **Portunus**, the system simulator developed by **Adapted Solutions**. In addition to the course materials, a number of example files are available. Customer-specific modelling problems may be discussed on demand.

